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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,120	12/30/2003	Alan Keith Bartky	134162	9796

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EXAMINER	
NGUYEN, PHUONGCHAU BA	
ART UNIT	**PAPER NUMBER**
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,120	BARTKY, ALAN KEITH	
	Examiner	Art Unit	
	Phuongchau Ba Nguyen	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-5, 9-18, 21 are rejected under 35 U.S.C. 102(a) as being anticipated by the admitted prior art (fig.1 as described in the Background of this present application).

Regarding claim 1,

The admitted prior art discloses a hierarchical multiplexing method comprising the steps of:

receiving a protocol data unit (PDU) associated with one of a plurality of flows (see fig.1, wherein PDU were received at 110 flows);

sequentially processing the PDU at each of a plurality of hierarchical levels (see page 2, line 19, wherein PDU were being processed from the first level of queues to the last), said processing at each of the plurality of hierarchical levels consisting of:

characterizing the flow at the current hierarchical level (page 2, lines 20-27); and

gating the PDU based upon the character of the flow at the current level (page 2, lines 20-27); and

outputting the PDU if the PDU is passed at each of the plurality of hierarchical levels (page 2, lines 20-27 and also see page 2, lines 13-16, outputting data at egress port).

Regarding claim 2, The admitted prior art further discloses wherein the plurality of hierarchical levels comprises a last hierarchical level (final level 108-fig.1),

wherein the step of sequentially processing the PDU at the last hierarchical level comprises the step of queuing the PDU (see also, page 2, lines 4-19).

Regarding claim 3, The admitted prior art further discloses wherein the step of queuing the PDU comprises the step of buffering the PDU at an egress queue (final queue 108-fig.1) associated with an egress port of a network switching device (see page 2, lines 13-15, the switch is not shown, but inherent therein, see page 1 lines 24-30).

Regarding claim 4, The admitted prior art further discloses wherein the step of queuing the PDU comprises the step of buffering the PDU preceding transmission to a switch fabric (see page 2, lines 13-19, buffering at the final queue 108) .

Regarding claim 5, The admitted prior art further discloses wherein the step of sequentially processing the PDU at one or more hierarchical levels comprises performing one or more forwarding operations (see fig.1, wherein all PDUs, that were received and not discarded, would be forwarded from first level of queues to the next level of queues, i.e., second level of queues, 105-107, fig.1).

Regarding claim 9, The admitted prior art further discloses wherein: characterizing comprises the step of measuring a flow rate for the flow associated with the PDU based on a current hierarchical level (page 2, lines 20-27); and gating comprises the step of discarding the PDU if it exceeds a maximum bandwidth parameter (page 2, lines 20-27).

Regarding claim 10, The admitted prior art discloses all the claimed limitations, except (1) wherein the gating comprises the steps of: associating with the PDU

a color marker using a three color marker algorithm; and applying discard control logic to selectively discard the PDU based upon the color marker.

However, in the same field of endeavor, Paatela (US2006/0209840A1) discloses a policer 711 having srTCM (single rate Tri-Color Marker) to discard the right packets based on the srTCM color marker, see 0094-0095, corresponding (1). Therefore, it would have been obvious to an artisan to apply Paatela's teaching to the admitted prior's system with the motivation being to provide a mechanism for marking packets when they exceed the contracted bandwidth to help manage network congestion at the output link and to allow the right packets to be discarded while facilitating fairness of resource usage.

Regarding claim 11,

The admitted prior discloses a hierarchical multiplexing method comprising the steps of:

receiving a protocol data unit (PDU) associated with one of a plurality of flows (see fig.1, wherein PDU were received at 110 flows);

sequentially processing the PDU at each of three or more hierarchical levels (see page 2, line 19, wherein PDU were being processed from the first level of queues to the last), said processing at each of the hierarchical levels comprising the step of gating the PDU (page 2, lines 20-27);

mapping the a plurality of flows between each of the hierarchical levels (page 2, lines 10 & 20-27); and

outputting the PDU if the PDU is passed at each of the plurality of hierarchical levels(page 2, lines 20-27 and also see page 2, lines 13-16, outputting data at egress port).

Regarding claim 12,

The admitted prior discloses a packet processing method comprising the steps of:

receiving a protocol data unit (PDU) associated with one of a plurality of flows (see fig.1, wherein PDU were received at 110 flows);

sequentially processing the PDU at each of a plurality of hierarchical levels (see page 2, line 19, wherein PDU were being processed from the first level of queues to the last), said processing at each of the plurality of hierarchical levels consisting of:

characterizing the flow at the current hierarchical level (page 2, lines 20-27); and

gating the PDU based upon the character of the flow at the current level (page 2, lines 20-27); and

outputting the PDU if the PDU is passed at each of the plurality of hierarchical levels (page 2, lines 20-27 and also see page 2, lines 13-16, outputting data at egress port).

Regarding claim 13,

The admitted prior art discloses a hierarchical multiplexor (fig.1) comprising:

an input channel (110-fig.1) for receiving a protocol data unit (PDU) associated with one of a plurality of flows;

a plurality of hierarchical levels (three levels of queues, 101-103, 105-107 and 108), each hierarchical level consisting of:

means for characterizing the flow at the hierarchical level (page 2, lines 20-27); and

means for gating the PDU based upon the character of the flow at the hierarchical level (page 2, lines 20-27); and

means for mapping the PDU to a flow at the next hierarchical level (page 2, lines 20-27, also see page 2, line 10); and

an output channel (i.e., egress port on to the output channel-not shown, would have been inherent for transmitting the output data from egress port) for

transmitting the PDU if the PDU is passed at each of the plurality of hierarchical levels.

Regarding claim 14, The admitted prior further discloses wherein one or more of the plurality of hierarchical levels further consists of means for performing forwarding operations associated with the PDU (see fig.1, wherein all PDUs, that were received and not discarded, would be forwarded from first level of queues to the next level of queues, i.e., second level of queues, 105-107, fig.1).

Regarding claim 15, The admitted prior further discloses wherein the hierarchical multiplexor further comprises a last hierarchical level (final queue 108-fig.1) comprising: means for characterizing the flow at the last hierarchical level (page 2, lines 20-27); and means for gating the PDU based upon the character of the flow at the last hierarchical level (page 2, lines 20-27).

Regarding claim 16, The admitted prior further discloses wherein the last hierarchical level (final queue 180-fig.1) further comprises a queue for buffering the PDU at the output channel (i.e., egress port on to the output channel-not shown, would have been inherent for transmitting the output data from egress port).

Regarding claim 17, The admitted prior further discloses wherein the means for characterizing the flow comprises a meter for measuring the flow rate of the flow associated with the PDU (page 2, lines 20-27).

Regarding claim 18, The admitted prior further discloses wherein the means for gating the PDU comprises means for discarding the PDU depending on the flow rate (page 2, lines 20-27).

Regarding claim 21,

The Admitted prior art (fig.1) discloses a hierarchical multiplexor (queue structure 100-fig.1) for processing a protocol data unit (PDU) associated with one of a plurality of flows (110-fig.1), the hierarchical multiplexor comprising:

a plurality of hierarchical levels (i.e., three levels, fig.1, wherein first level of queues 101-103, second level of queues 105-107, and third/final level of queue 108) for performing gating operations (i.e., passing), each hierarchical level consisting of:

a meter for measuring the flow rate at the hierarchical level (page 2, lines 20-27; and

a gate for discarding the PDU based upon the flow rate at the hierarchical level (page 2, lines 20-27); and

a last hierarchical level (i.e., the final level, fig.1) comprising a queue (108-fig.1) for buffering the PDU prior to transmission.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art as applied to claim 1 above, and further in view of Fine (6,813,250).

Regarding claims 6 and 8, The admitted prior art all the claimed limitations, except (1) wherein the one or more forwarding operations comprise appending an address to the PDU (claim 6); (2) appending one or more virtual local area network (VLAN) tags at one or more hierarchical levels.

However, in the same field of endeavor, Fine (6,813,250) discloses appending source/destination address 332 &334 to header 302 for forwarding

the PDU packet to the next interconnect switch, see col.9, line 63-col.10, line 2), corresponding to (1) and VLAN tag to the PDU packet/frame, see figs. 3A-3B, corresponding (2). Therefore, it would have been obvious to an artisan to apply Fine's teaching to the admitted prior's system with the motivation being to only append the address upon necessity to reserve the packet length in transition.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Fine as applied to claim 6 above, and further in view of Nogami (6,781,994).

Regarding claim 7, The admitted prior art all the claimed limitations, except (1) wherein the appending of an address to the PDU comprises the steps of: appending a virtual circuit identifier at a first hierarchical level; and appending a virtual path identifier at a second hierarchical level.

However, in the same field of endeavor, Nogami (6,781,994) discloses appending new VPI/VCI header to PDU that is corresponding to the next output destination (NEXT HOP) to that data in place of an old one, see col.23, line 66-col.24, line 7. Therefore, it would have been obvious to an artisan to apply Nogami's teaching to the admitted prior art with the motivation being to only forward data to next hop as to only append the valid PDU packet with a new VCI/VPI header to the next hop to help manage congestion in the switching network.

6. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art as applied to claim13 above, and further in view of Paatela (US2006/0209840A1).

Regarding claim 19, The admitted prior all the claimed limitations, except (1) wherein the means for characterizing the flow further comprises a marker

module for marking the PDU in accordance with a Three-Color Marker (TCM) algorithm.

However, in the same field of endeavor, Paatela (US2006/0209840A1) discloses a policer 711 having srTCM (single rate Tri-Color Marker), see 0094-0095, corresponding (1). Therefore, it would have been obvious to an artisan to apply Paatela's teaching to the admitted prior's system with the motivation being to provide a mechanism for marking packets when they exceed the contracted bandwidth to help manage network congestion at the output link and to allow the right packets to be discarded while facilitating fairness of resource usage.

Regarding claim 20, Paatela further discloses wherein the means for gating the PDU comprises means for discarding the PDU in accordance with the TCM algorithm, see 0094-0095, the motivation for combining the Patatela and the admitted prior is set forth in claim 19.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuongchau Ba Nguyen whose telephone number is 571-272-3148. The examiner can normally be reached on Monday-Friday from 10:00 a.m. to 6:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PChau

Phuongchau Ba Nguyen
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